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EXAMINER
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GOUDREAU, GEORGE A

ART UNIT	PAPER NUMBER
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1763

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09-774,323

Applicant(s)

Campbell et al.

Examiner

George Goudreau

Group Art Unit

1763

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- ☒ Responsive to communication(s) filed on 1-31-01 (ie. - paper #1)
- ☐ This action is FINAL.
- ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- ☒ Claim(s) 1-20 is/are pending in the application.
- ☐ Of the above claim(s) is/are withdrawn from consideration.
- ☐ Claim(s) is/are allowed.
- ☒ Claim(s) 1-20 is/are rejected.
- ☐ Claim(s) is/are objected to.
- ☐ Claim(s) are subject to restriction or election requirement

## Application Papers

- ☐ The proposed drawing correction, filed on \_\_\_\_\_ is ☐ approved ☐ disapproved.
- ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119 (a)-(d)

- ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).
- ☐ All ☐ Some\* ☐ None of the:
- ☐ Certified copies of the priority documents have been received.
- ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_
- ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

\*Certified copies not received: \_\_\_\_\_

## Attachment(s)

- ☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). \_\_\_\_\_
- ☒ Notice of Reference(s) Cited, PTO-892
- ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☐ Interview Summary, PTO-413
- ☐ Notice of Informal Patent Application, PTO-152
- ☐ Other \_\_\_\_\_

Office Action Summary

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 5-12, 14, and 16-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsai (5,981,353).

Tsai discloses several different processes for forming an STI structure (106) on the front face of a CZ-Si wafer (100).

In a first embodiment they employ the following sequence of process steps:

- A pad SiO<sub>2</sub> layer (101, 101') is grown on both faces of the wafer (100).;
- A Si<sub>3</sub>N<sub>4</sub> layer (102, 102') is grown on the SiO<sub>2</sub> pad layers.;
- An STI trench (103) is etched into the front face of the wafer using a combination of a photolithography step , and etching steps.;
- A sidewall oxide layer (104) is grown inside the trench etched in the front face of the wafer. Simultaneously, an oxide is grown on the surface of the second Si<sub>3</sub>N<sub>4</sub> layer.;
- TEOS is used fill the STI trench.;
- The second oxide layer on the second Si<sub>3</sub>N<sub>4</sub> layer is removed in an HF wet etch step.;
- The TEOS layer is cmp planarized down to the surface of the Si<sub>3</sub>N<sub>4</sub> polishing stop layer.;
- and
- The Si<sub>3</sub>N<sub>4</sub> layer on the first, and the second faces of the wafer is the removed in a H<sub>3</sub>PO<sub>4</sub> wet etching step.

This is discussed specifically in columns 2-6; and discussed in general in columns 1-8.

This is shown in figures 1-7.

3. Claims 1-2, 8, 10-13, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Burns et. al. (5,738,757).

Burns et. al. disclose a process for the multi-depth etching of a silicon wafer which is comprised of the following steps:

- A SiO<sub>2</sub> layer (12) is formed onto both faces of a Si wafer (10).;
- A Si<sub>3</sub>N<sub>4</sub> layer (14) is formed onto both SiO<sub>2</sub> layers (12).;
- A SiO<sub>2</sub> layer (16) is formed onto both Si<sub>3</sub>N<sub>4</sub> layers (14).;
- A Si<sub>3</sub>N<sub>4</sub> layer (18) is formed onto both SiO<sub>2</sub> layers (16).;
- The Si<sub>3</sub>N<sub>4</sub> layers (18)/ SiO<sub>2</sub> layers (16) are patterned on both faces of the wafer using a photo lithographic step in combination with etching steps. A Si<sub>3</sub>N<sub>4</sub> etchant is used to first etch the Si<sub>3</sub>N<sub>4</sub> layers followed by the usage of a SiO<sub>2</sub> etchant to etch the SiO<sub>2</sub> layers.;
- The Si<sub>3</sub>N<sub>4</sub> layers (14) is patterned, and etched using a third etching step in combination with a second photolithography step.;
- The SiO<sub>2</sub> layers (12) is patterned, and etched using a fourth etching step in combination with a third photolithography step.;
- The Si is wet etched in KOH using the patterned Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> layers as an etch mask.

This is discussed specifically in columns 4-12; and discussed in general in columns 1-18.

This is shown in figures 1-8.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai as applied in paragraph 2 above.

Tsai as applied in paragraph 2 above fail to specifically disclose the formation of the Si<sub>3</sub>N<sub>4</sub> layer to the specific thicknesses which are claimed by the applicant.

It would have been obvious to one skilled in the art to form the Si<sub>3</sub>N<sub>4</sub> layers in the process taught above to the specific thicknesses which are claimed by the applicant based upon the following. It would have been desirable to form the Si<sub>3</sub>N<sub>4</sub> layers in the process taught above such that an adequate level of thickness is provided to properly construct the STI device without using an excessively thick layer of Si<sub>3</sub>N<sub>4</sub> which would undesirably waste process time, and undesirably increase processing costs.

7. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et. al. as applied in paragraph 3 above.

Burns et. al. as applied in paragraph 3 above fail to disclose the following aspects of applicant's claimed invention:

- the specific usage of a H<sub>3</sub>PO<sub>4</sub> wet etch step to pattern the Si<sub>3</sub>N<sub>4</sub> layer in the process taught above; and
- the specific formation of the Si<sub>3</sub>N<sub>4</sub> layers in the process taught above to the specific thicknesses which are claimed by the applicant

It would have been obvious to one skilled in the art to use a H<sub>3</sub>PO<sub>4</sub> wet etch step to pattern any of the Si<sub>3</sub>N<sub>4</sub> layers in the process taught above based upon the following. The usage of a H<sub>3</sub>PO<sub>4</sub> wet etch step to pattern a Si<sub>3</sub>N<sub>4</sub> layer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for patterning the Si<sub>3</sub>N<sub>4</sub> layers in the process taught above to the specific means which are taught above.

It would have been obvious to one skilled in the art to form the Si<sub>3</sub>N<sub>4</sub> layers in the process taught above to the specific thicknesses which are claimed by the applicant based upon the following. It would have been desirable to form the Si<sub>3</sub>N<sub>4</sub> layers to an adequate thickness for the function of these layers (i.e.-an etch mask) without forming the Si<sub>3</sub>N<sub>4</sub> layers to an excessive thickness which would undesirably waste process time, and money

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner George A. Goudreau whose telephone number is (703) -308-1915. The examiner can normally be reached on Monday through Friday from 9:30 to 6:00.

Art Unit: 1763

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Examiner Gregory Mills, can be reached on (703) -308-1633. The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) -306-3186.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) -308-0661.



George A. Goudreau/gag

Primary Examiner  
AU 1763